ABSTRACT OF THE DISCLOSURE

In one embodiment, a memory controller is coupled to a memory subsystem and controls accesses to the memory subsystem. In addition, a temperature sensor is positioned to detect a temperature associated with the memory subsystem. In this embodiment, the memory controller is configured to selectively insert one or more idle clock cycles between a first memory access and a second memory access depending upon the sensed temperature. In a further embodiment, a sensor is positioned to detect a power condition associated with the memory subsystem. In this embodiment, the memory controller is configured to selectively insert one or more idle clock cycles between a first memory access and a second memory access depending upon the detected power condition.